

FIG. 1

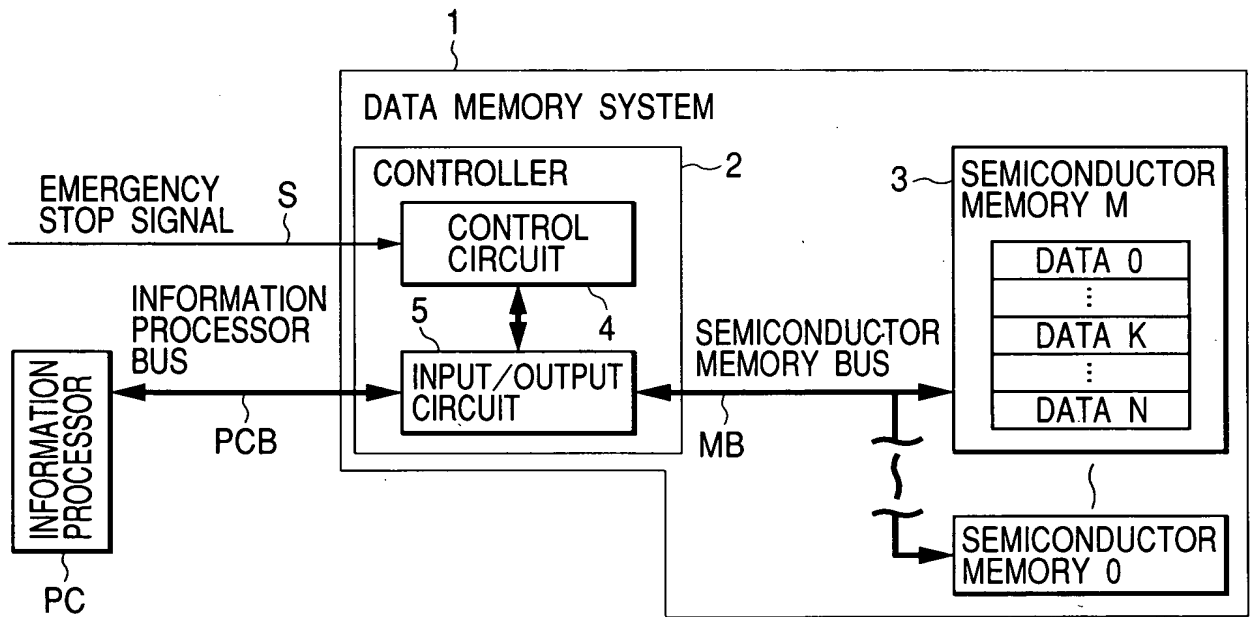


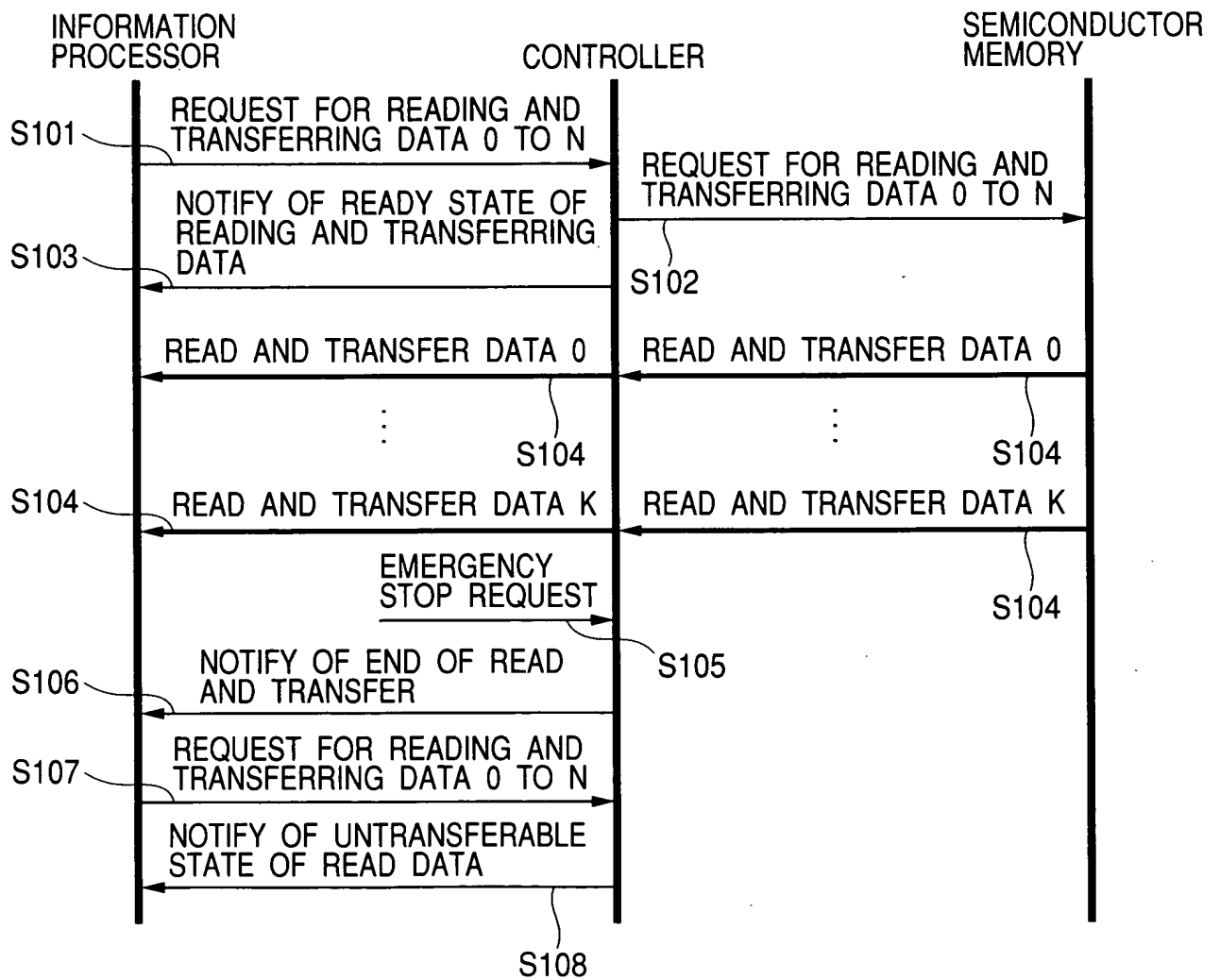
FIG. 2

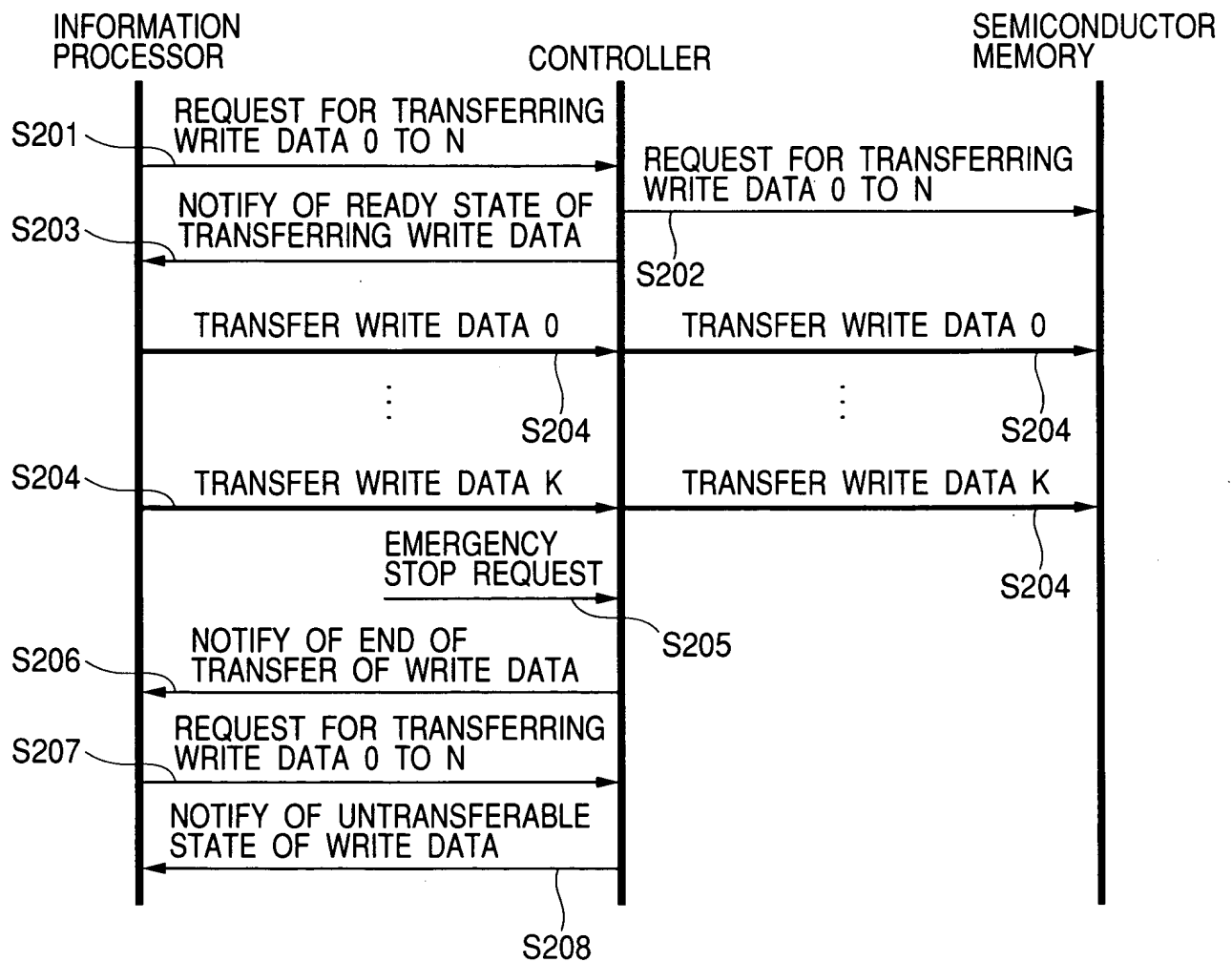
FIG. 3

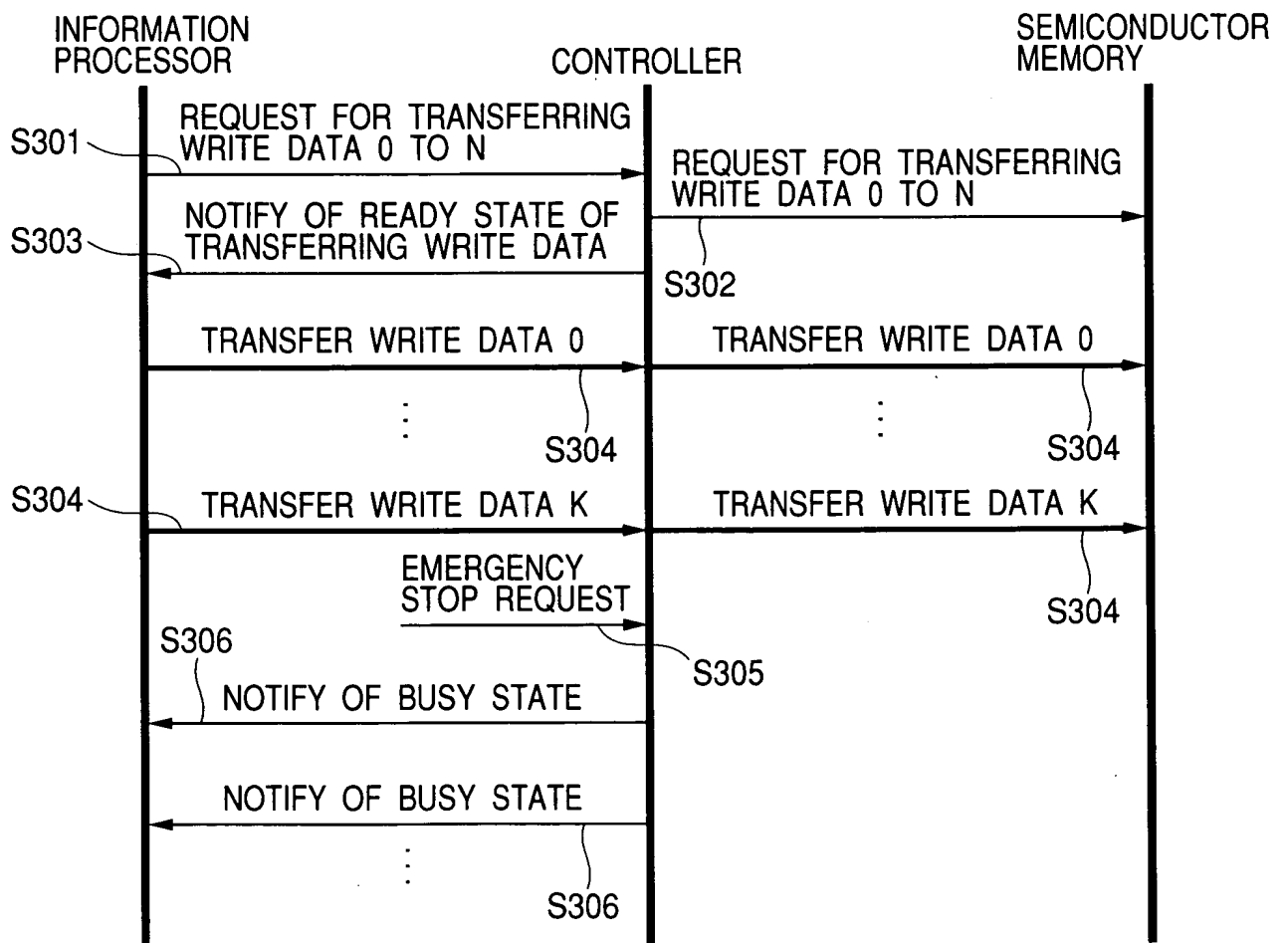
FIG. 4

FIG. 5

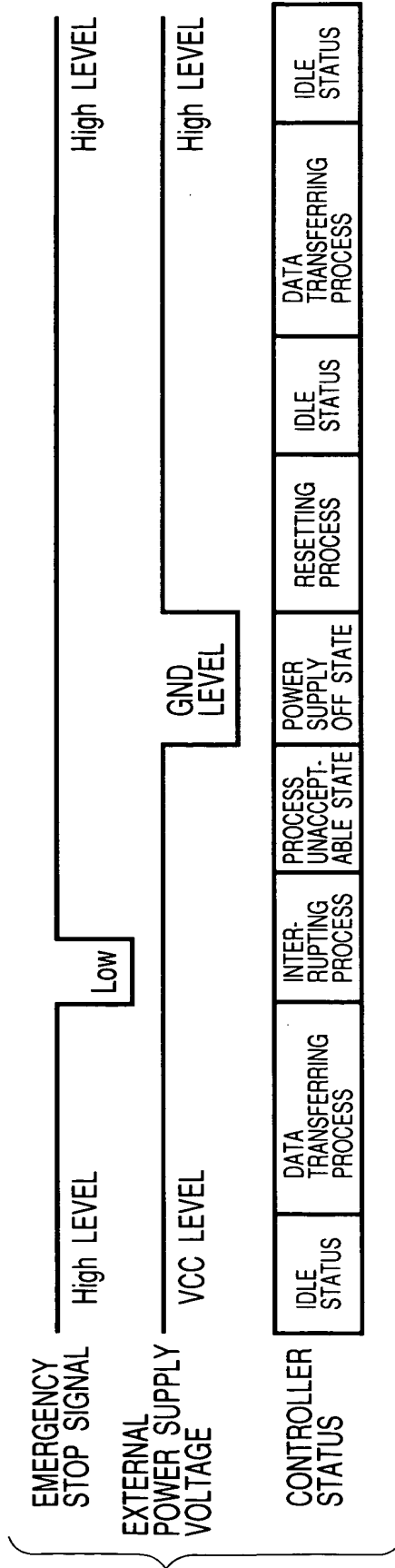


FIG. 6

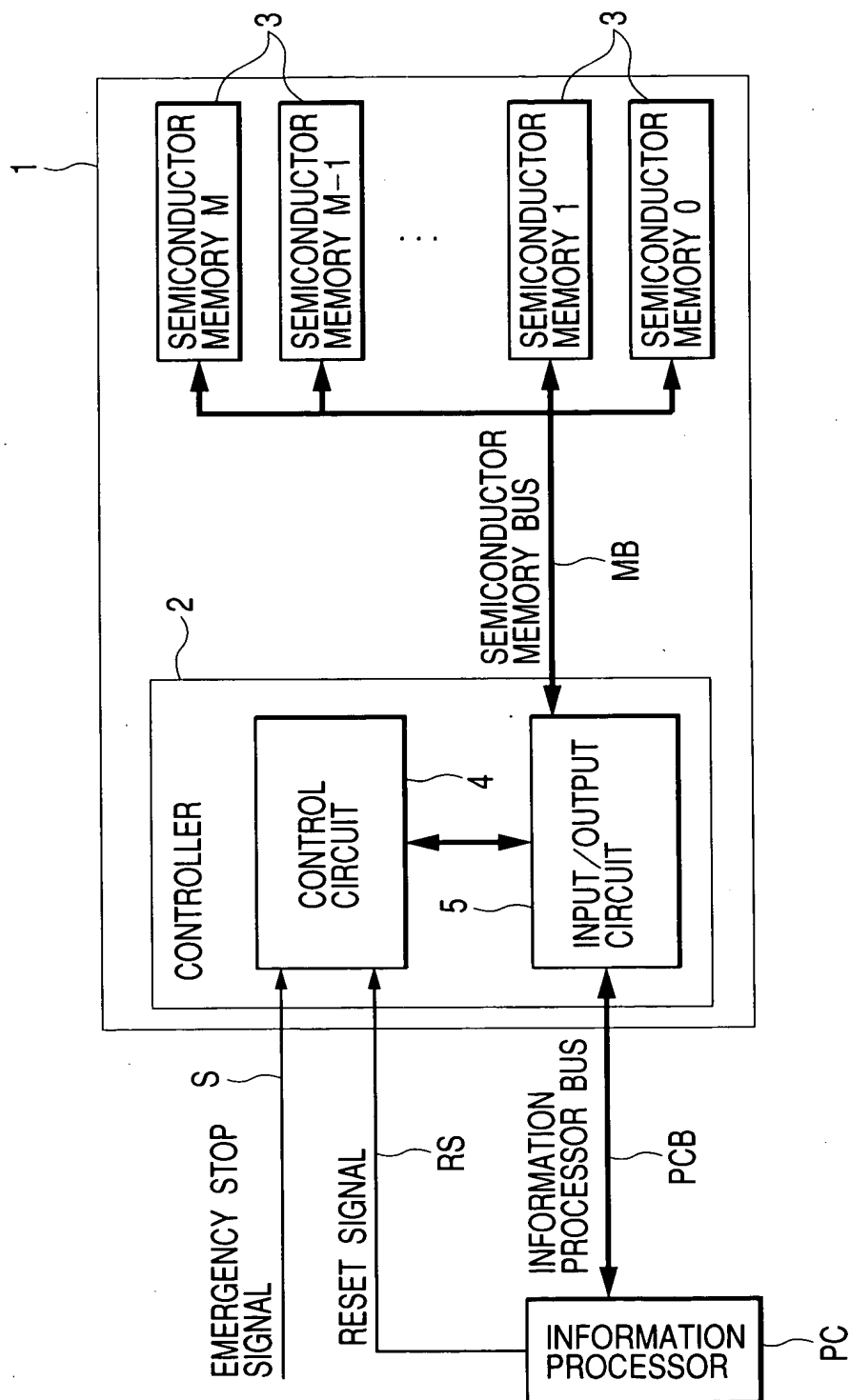


FIG. 7

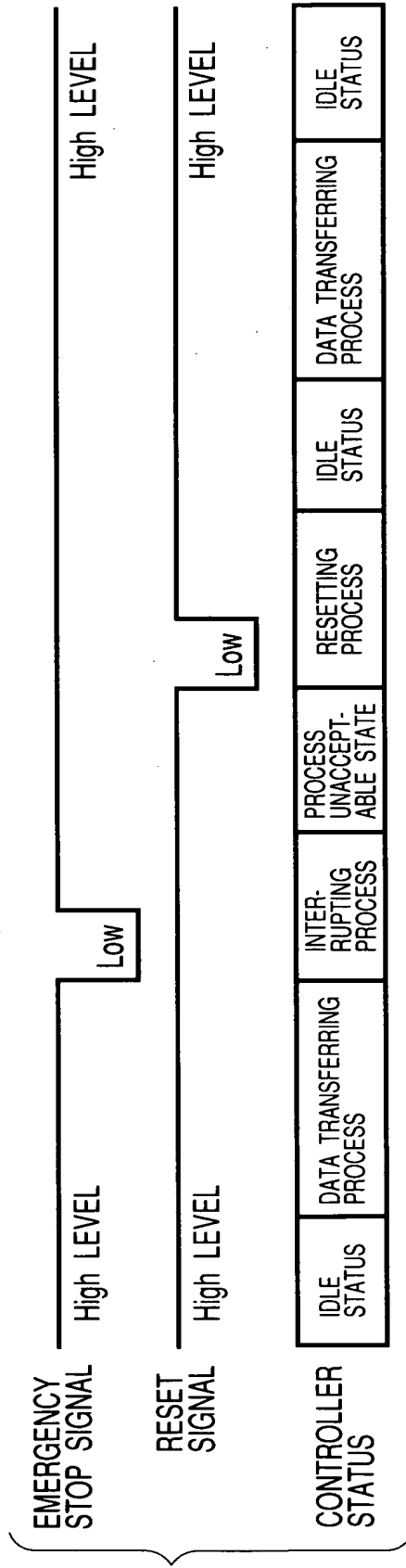


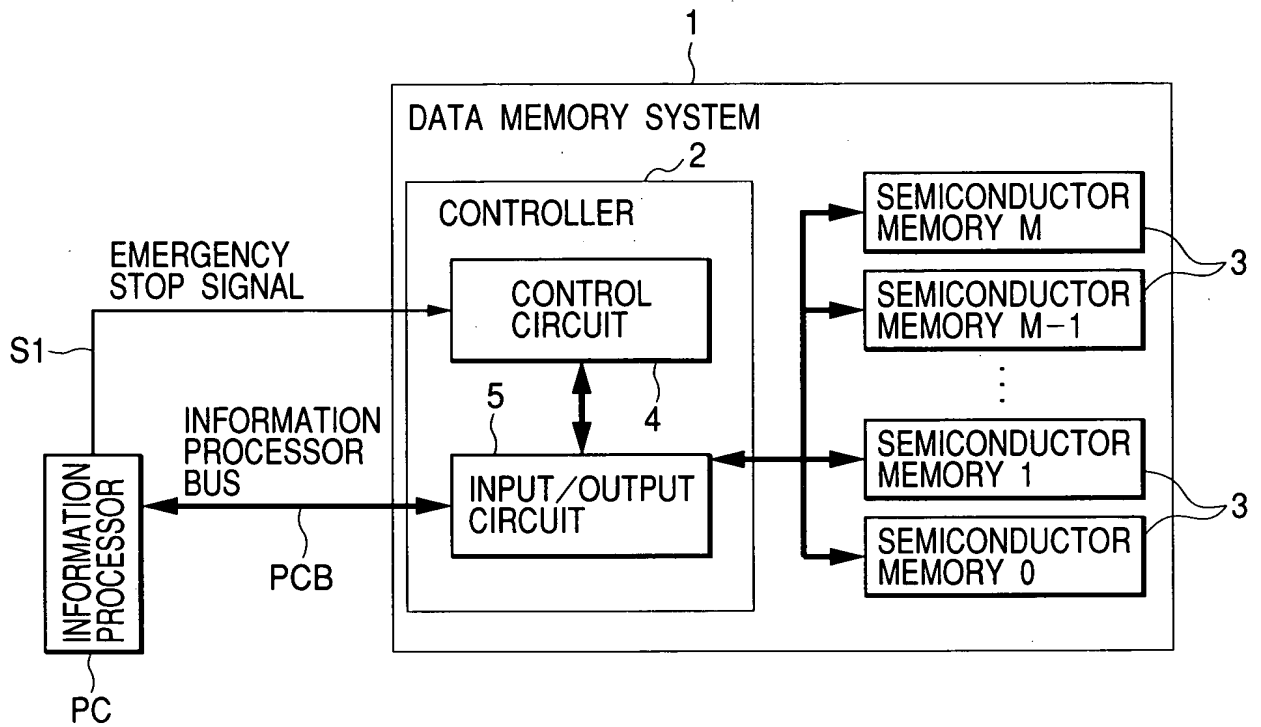
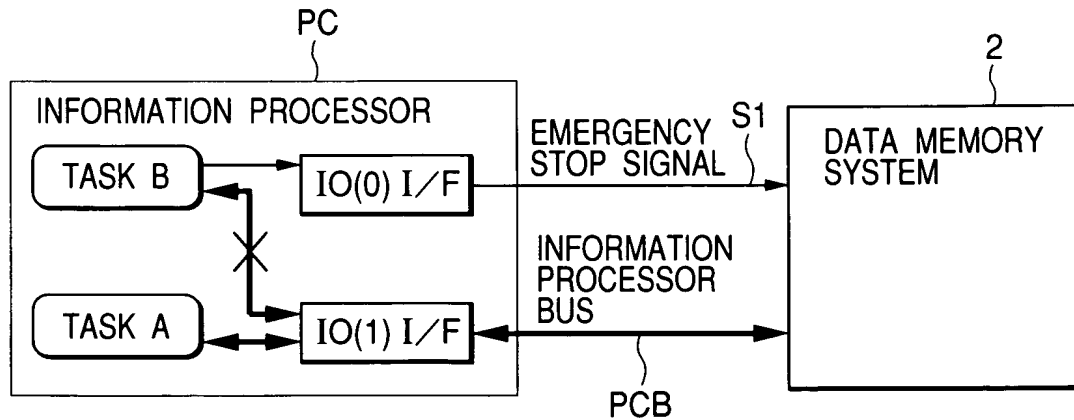
FIG. 8**FIG. 9**

FIG. 10

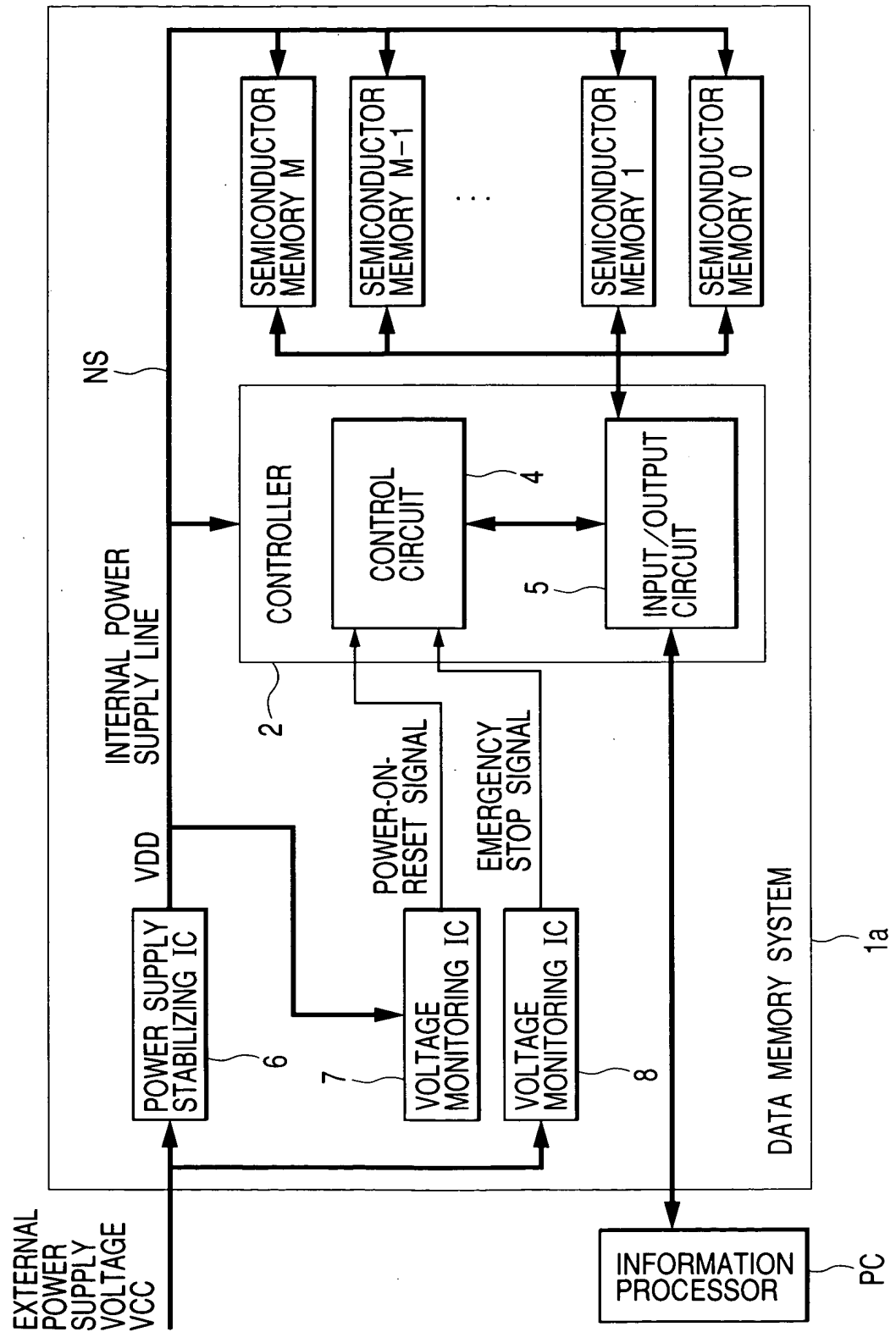


FIG. 12

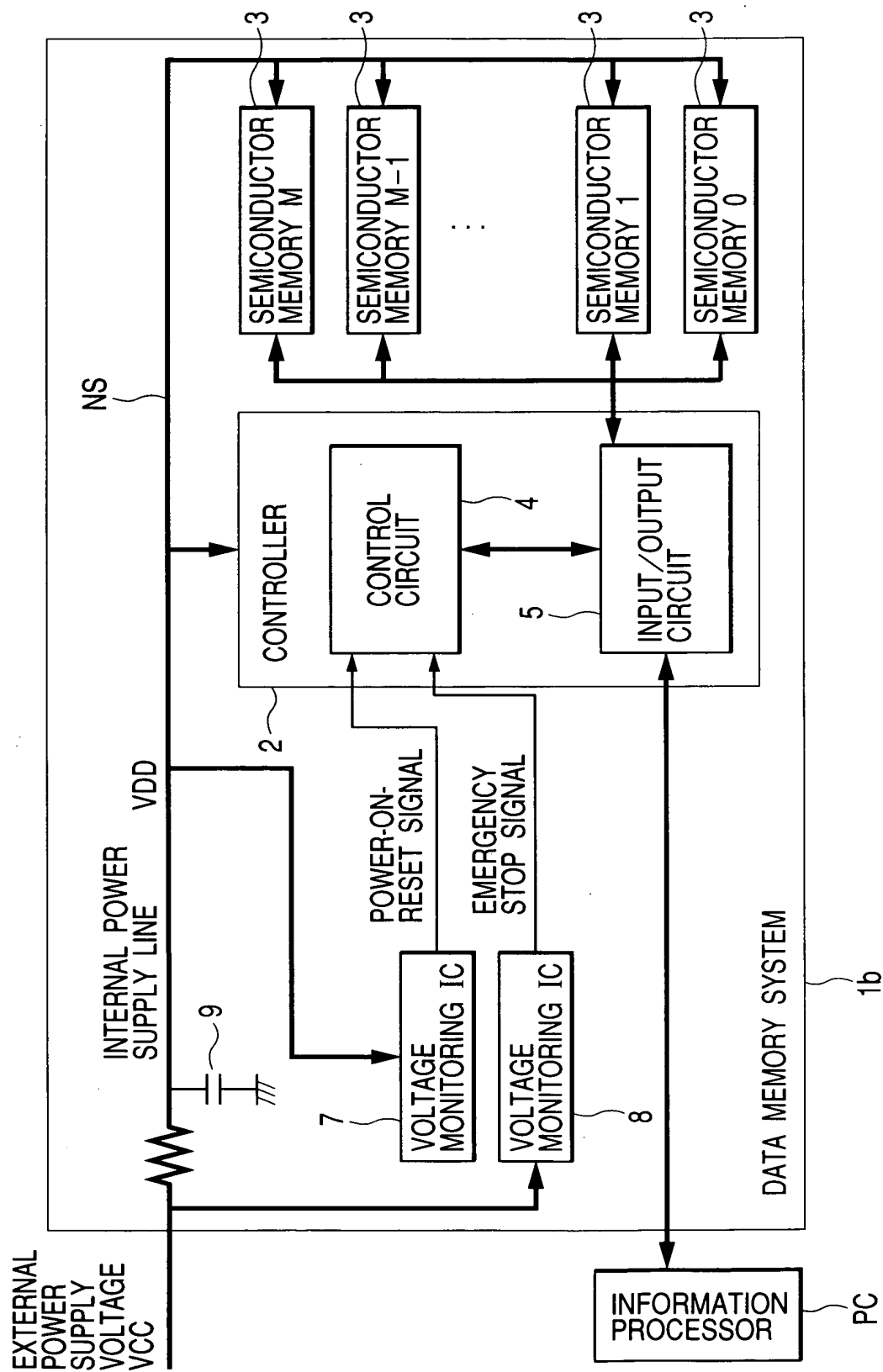


FIG. 13

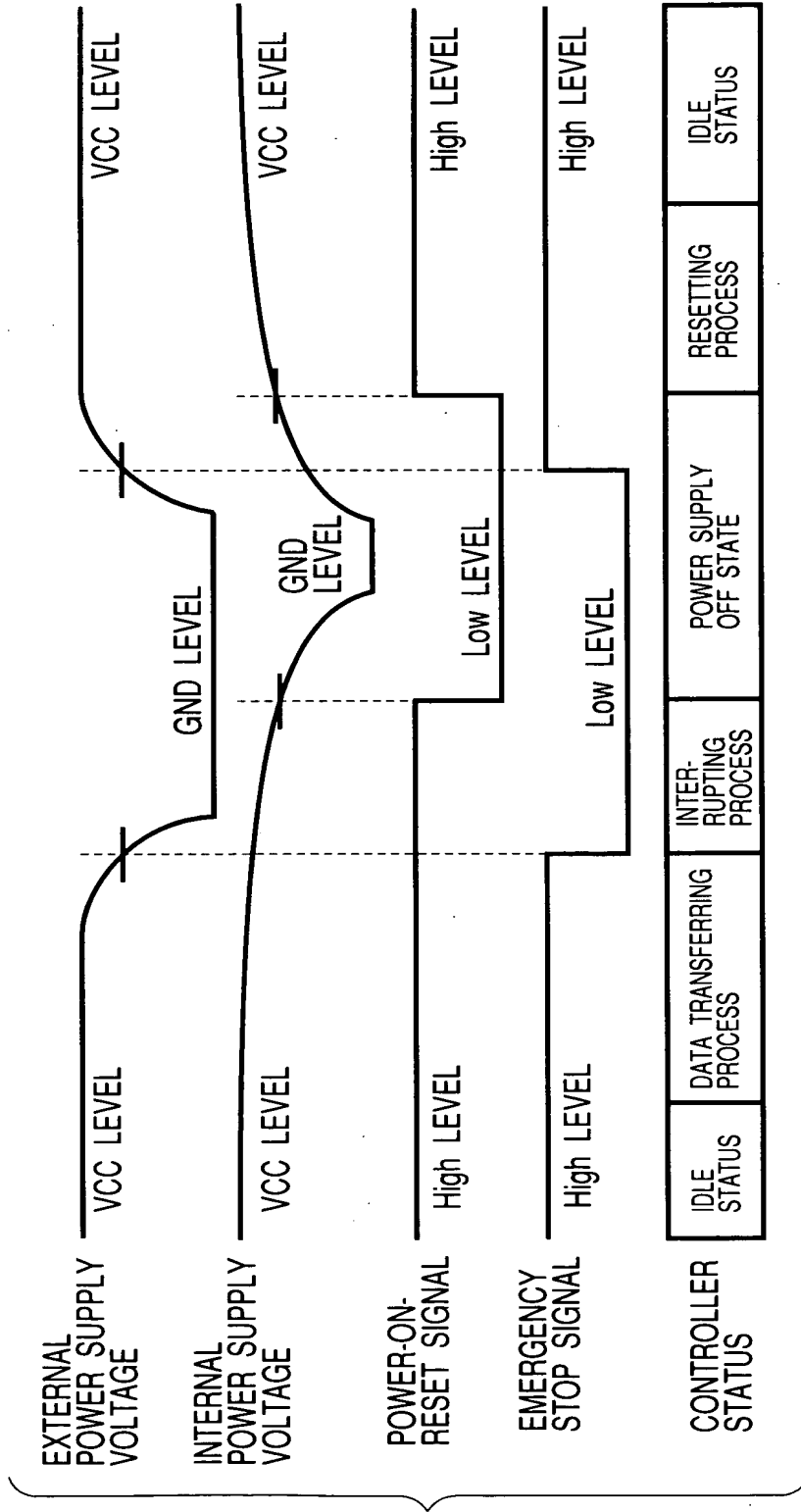


FIG. 14

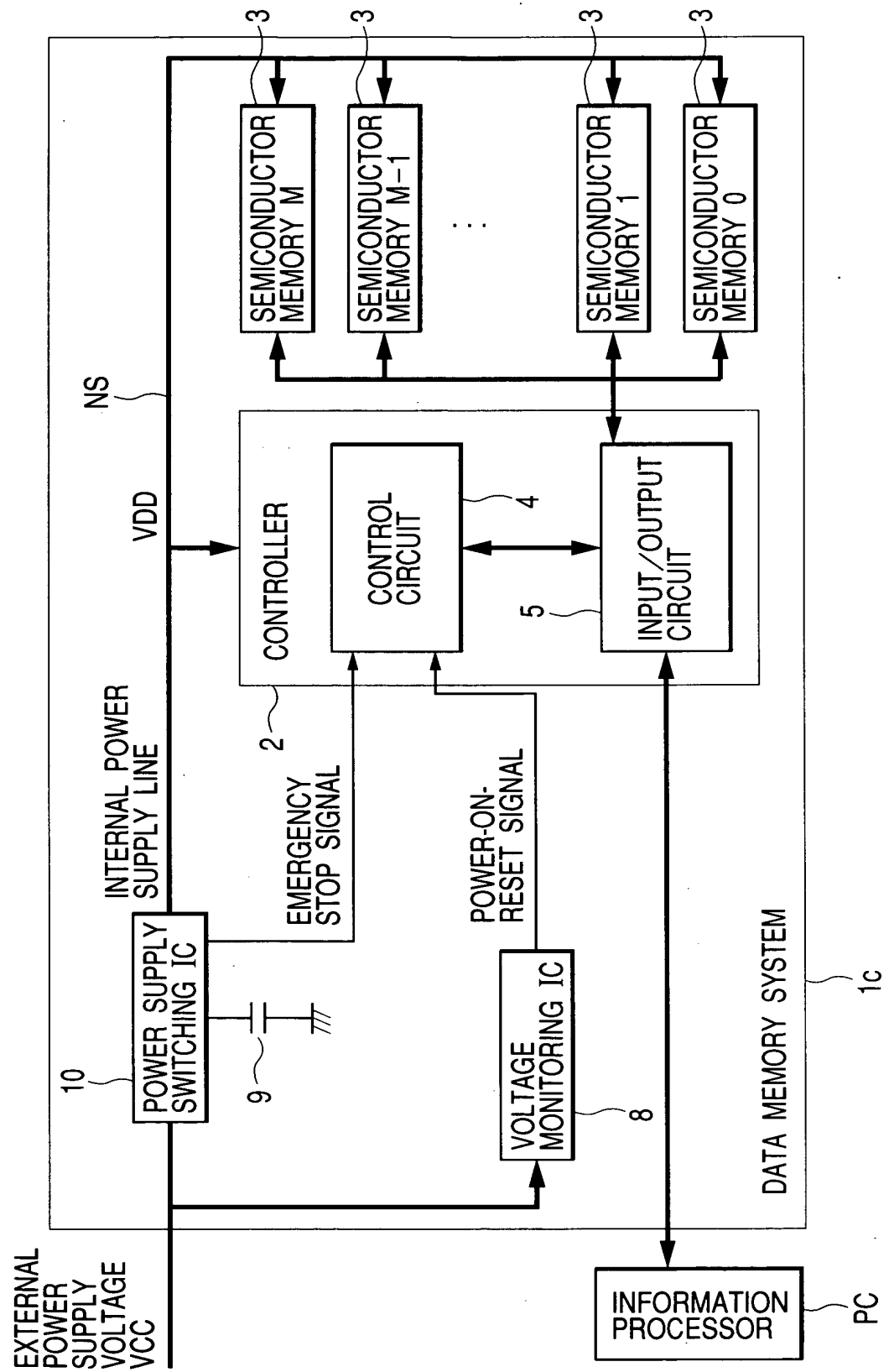


FIG. 15

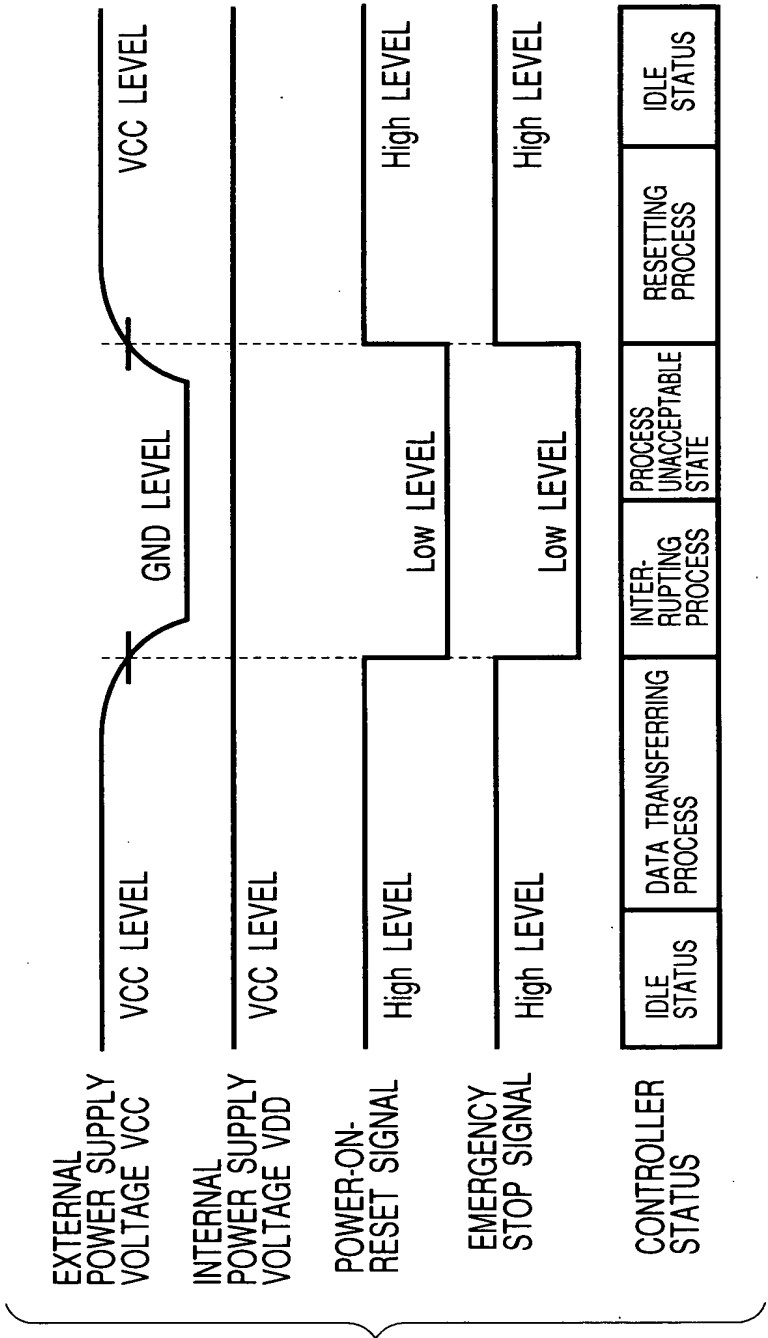


FIG. 16

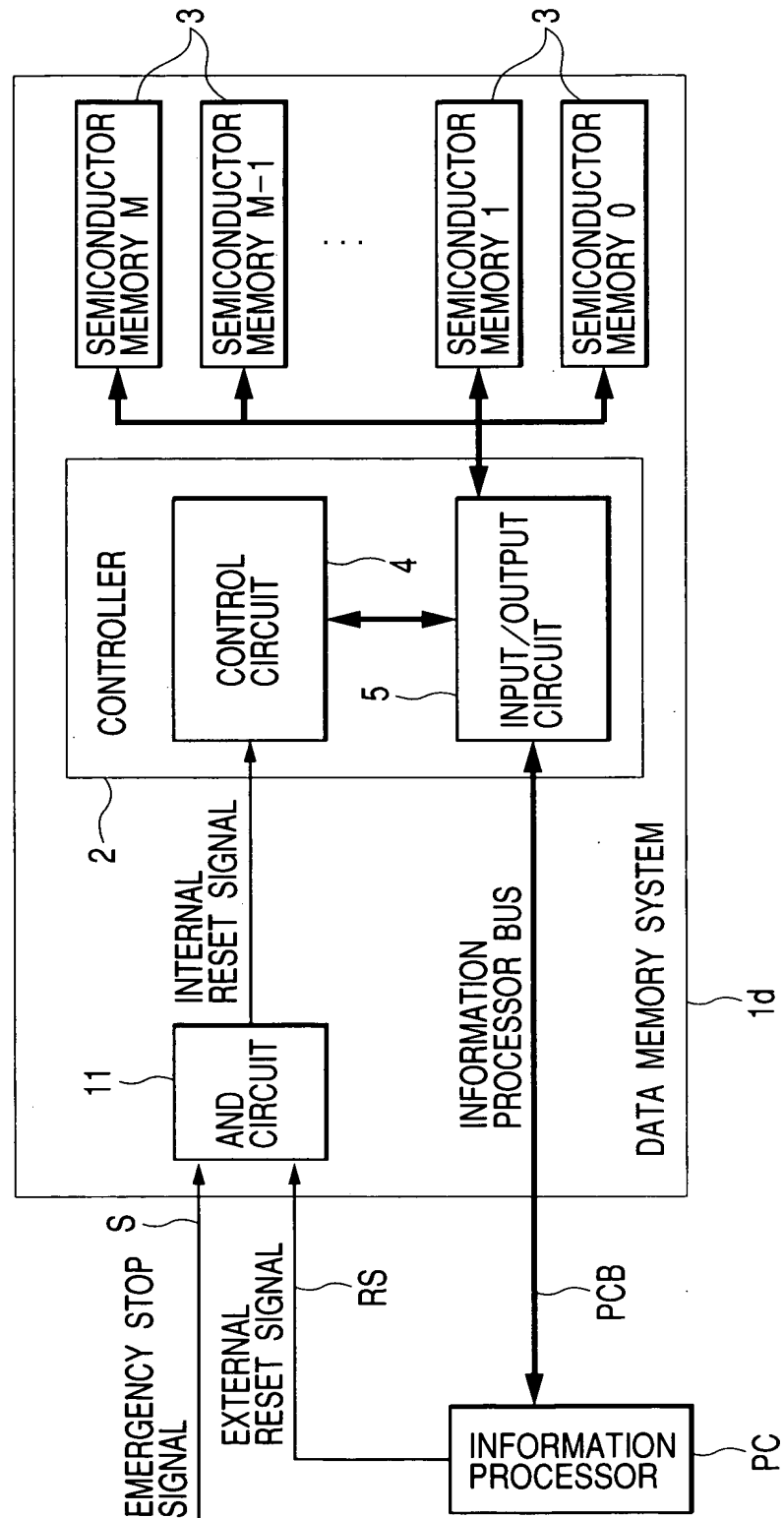


FIG. 17

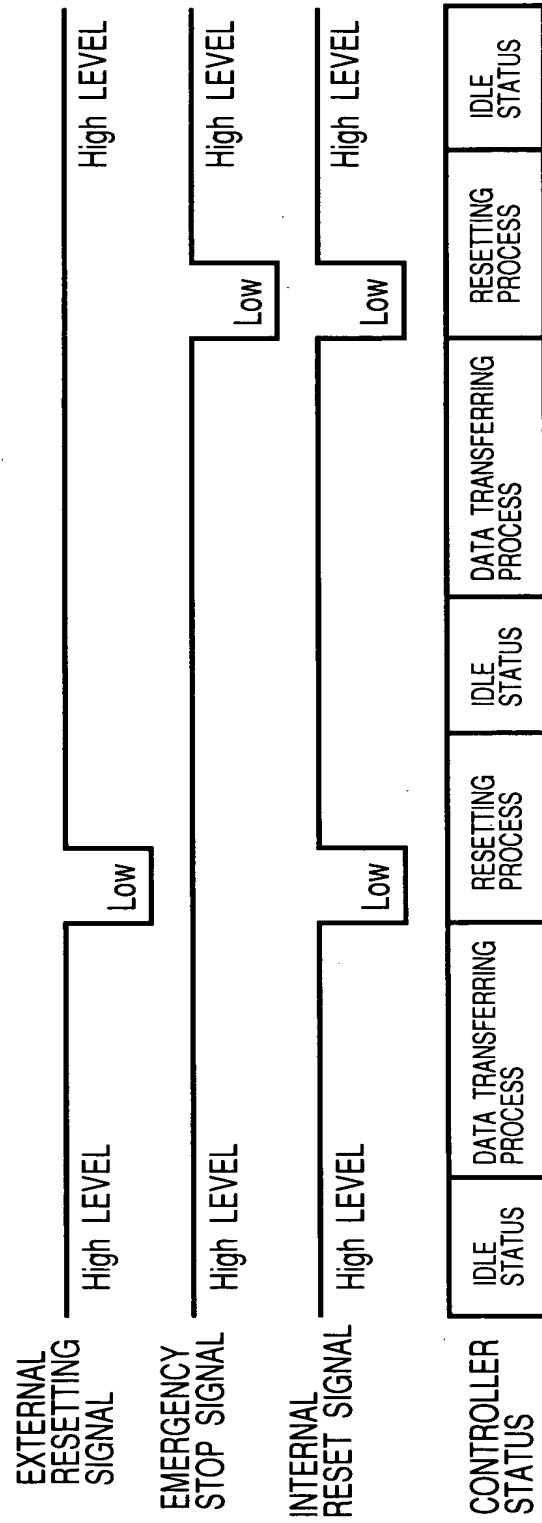
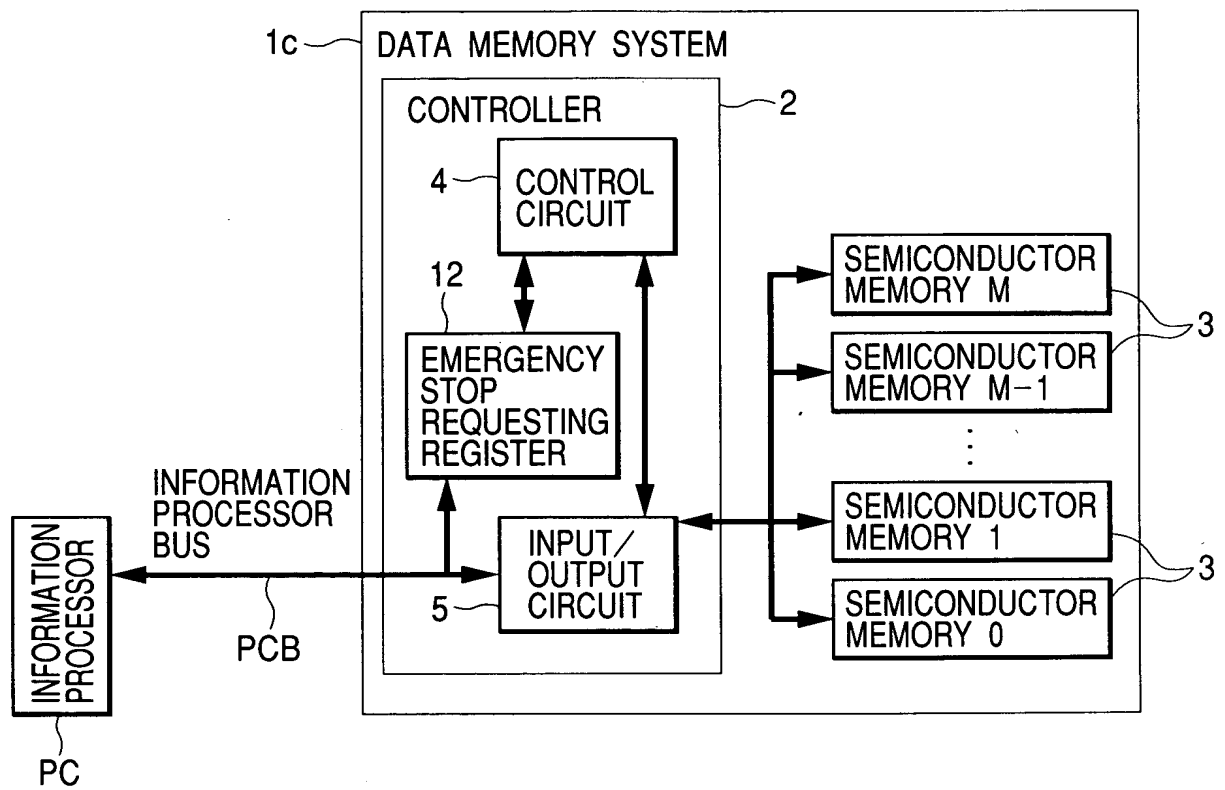
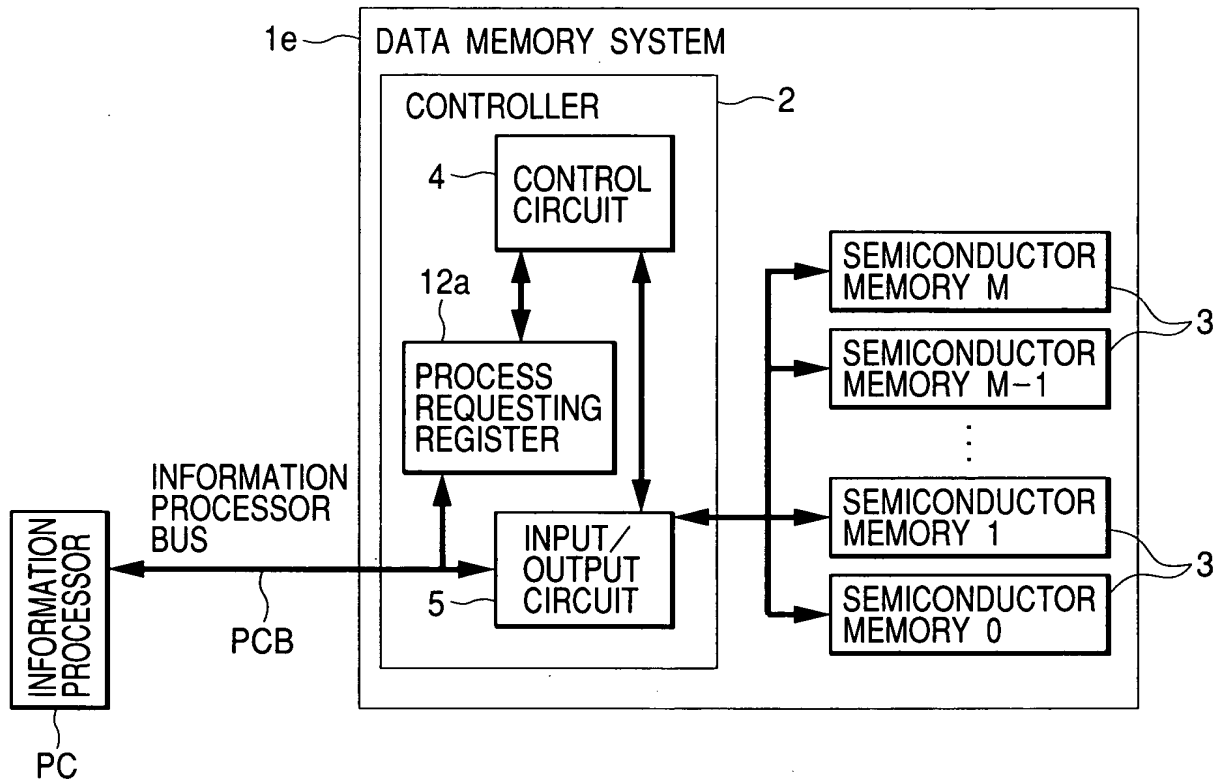
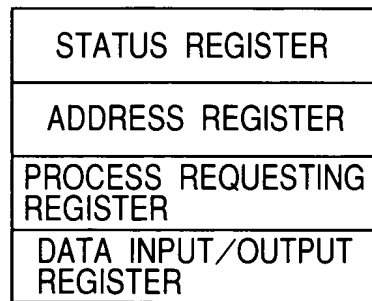


FIG. 18**FIG. 19**

EMERGENCY STOP REQUESTING REGISTER
STATUS REGISTER
ADDRESS REGISTER
PROCESS REQUESTING REGISTER
DATA INPUT/OUTPUT REGISTER

FIG. 20**FIG. 21**

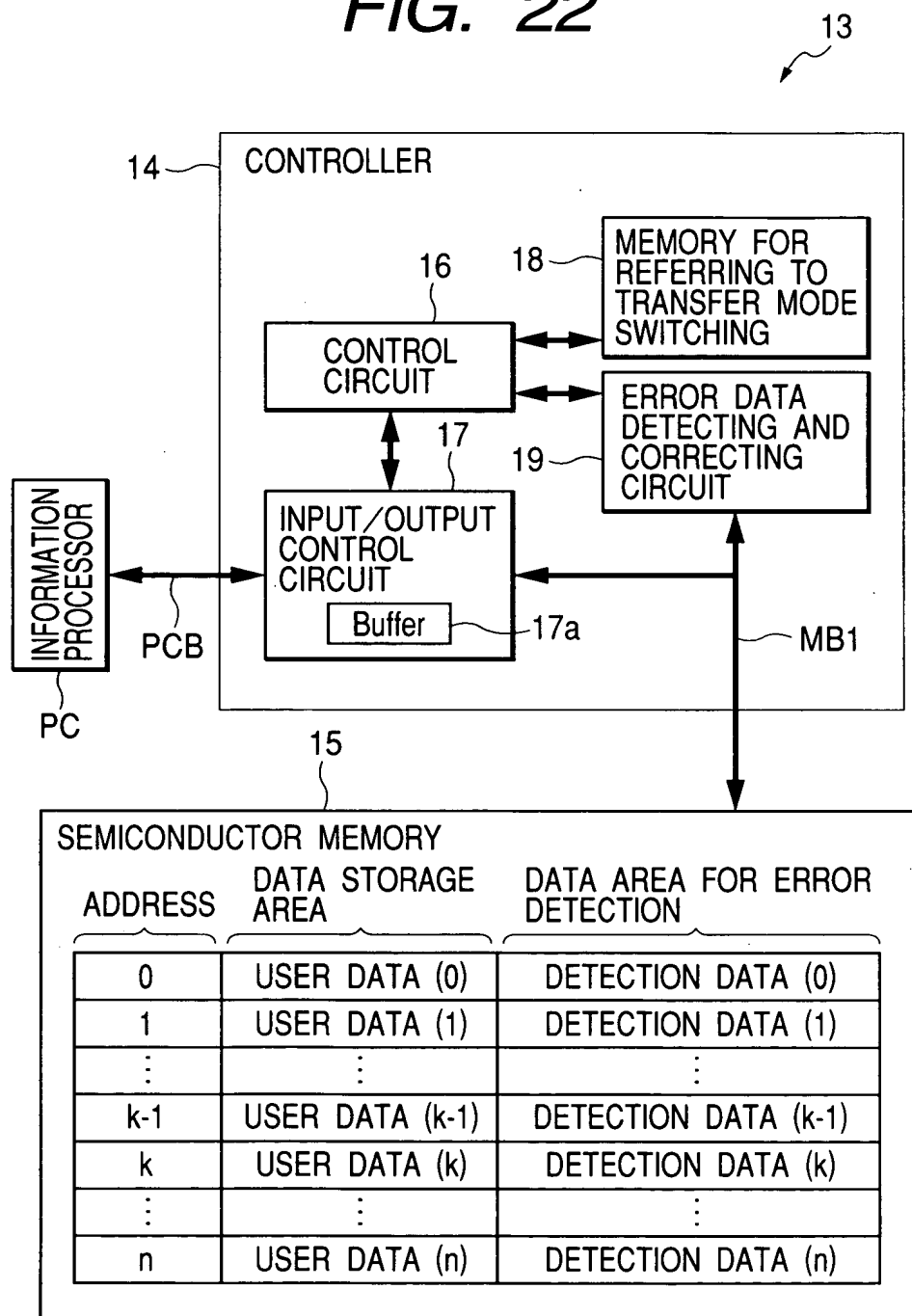


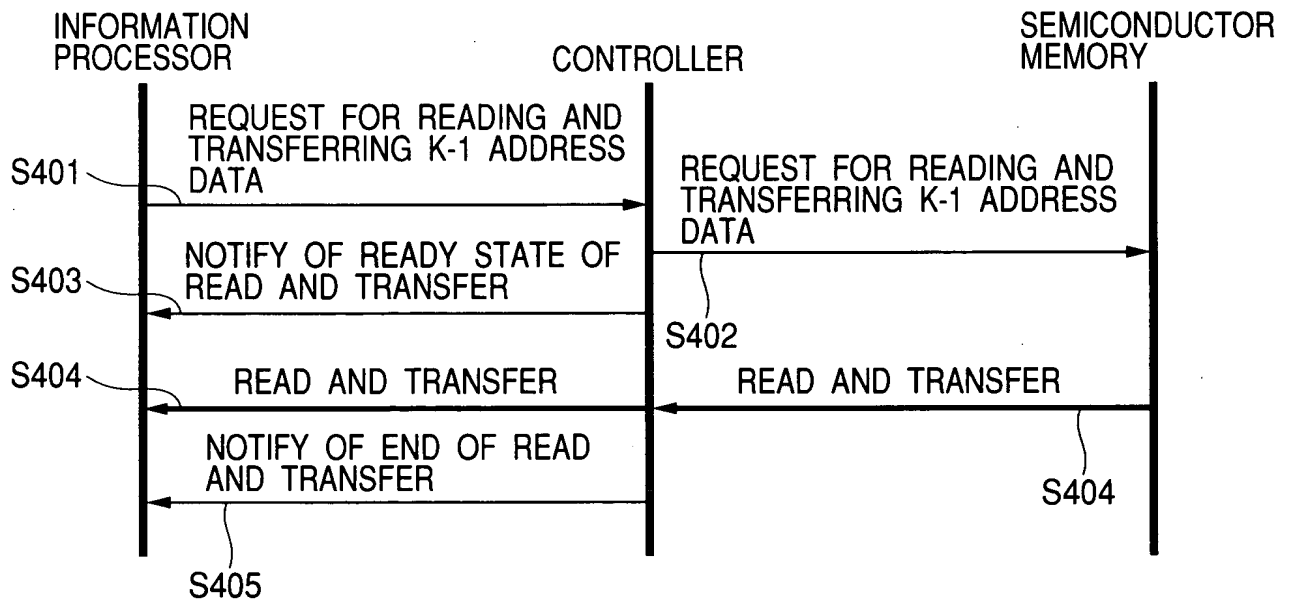
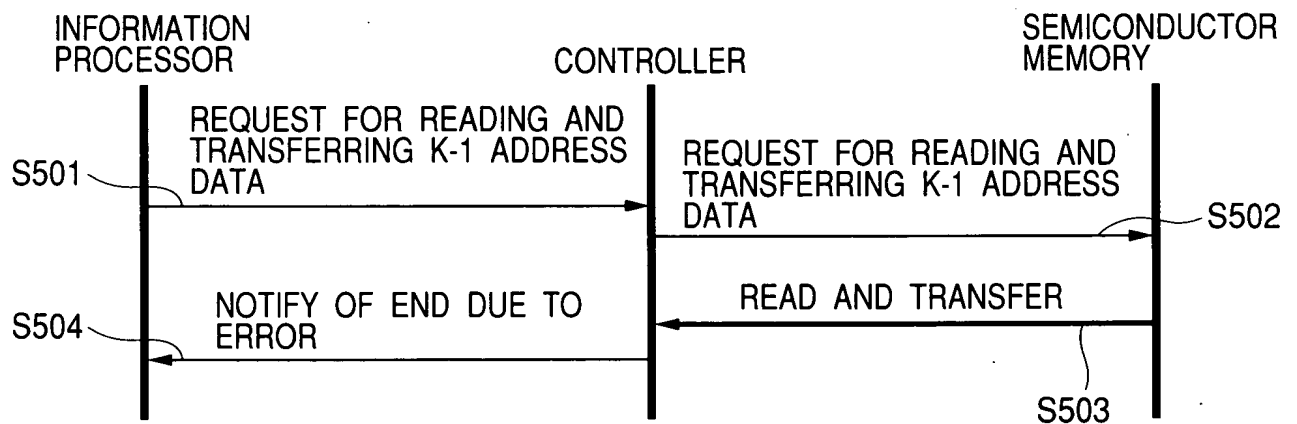
FIG. 23**FIG. 24**

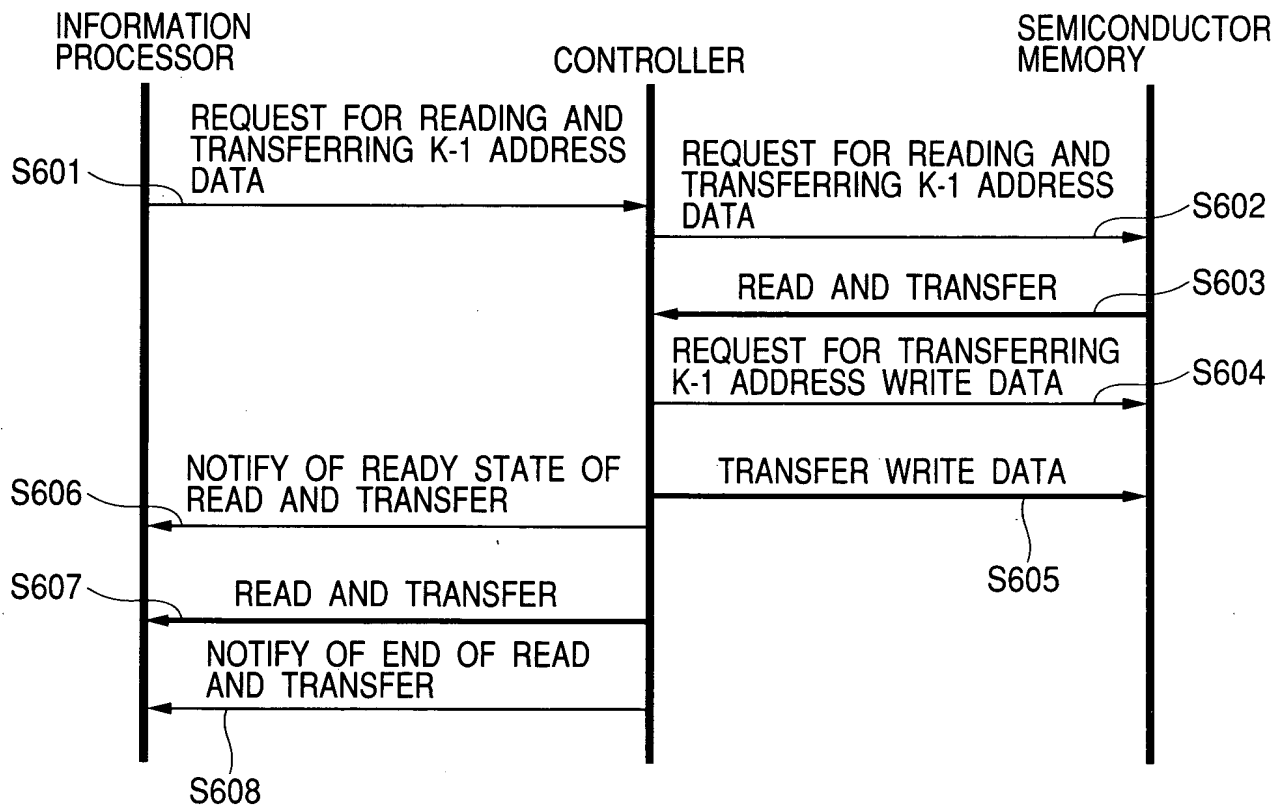
FIG. 25

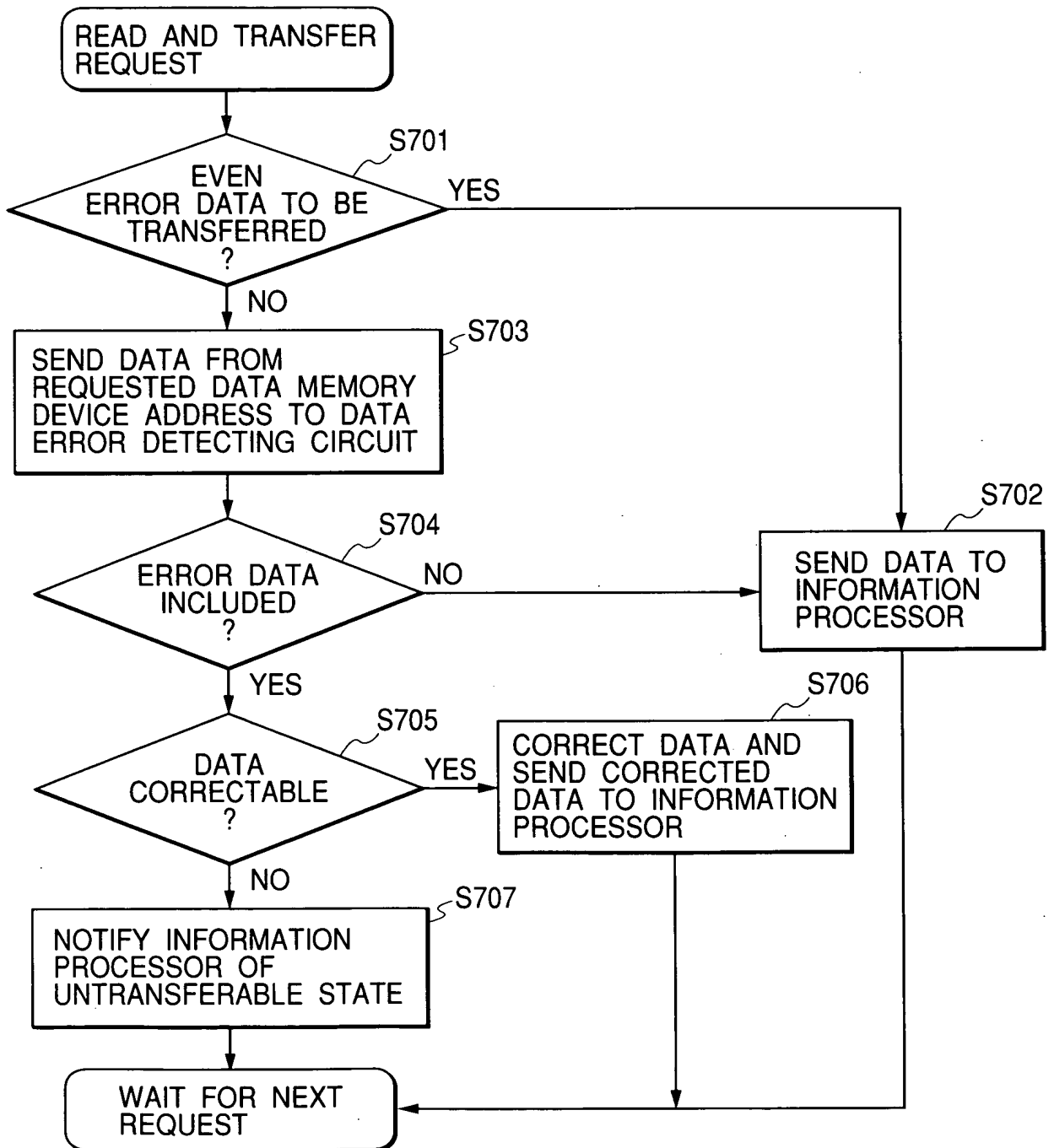
FIG. 26

FIG. 27

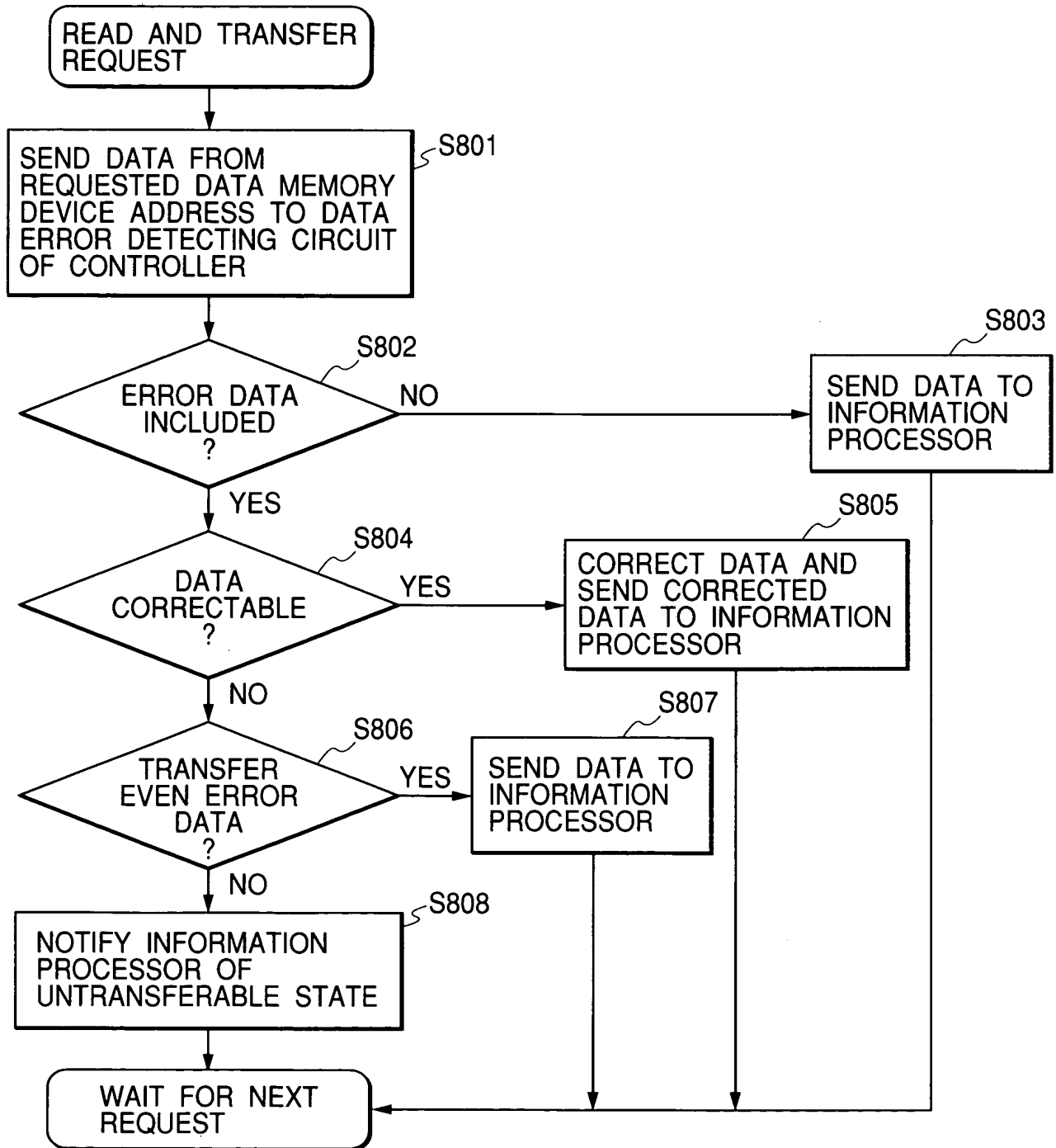


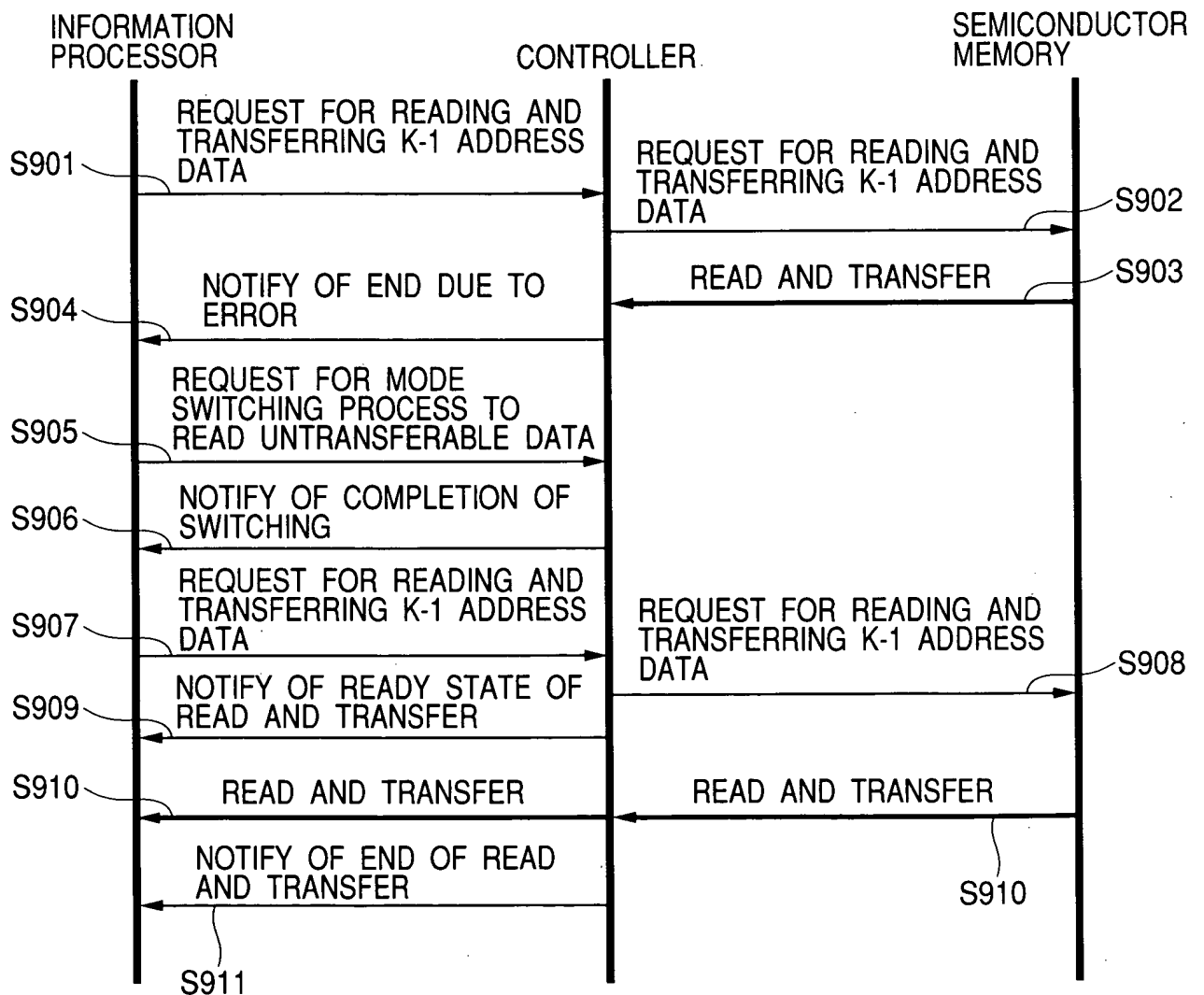
FIG. 28

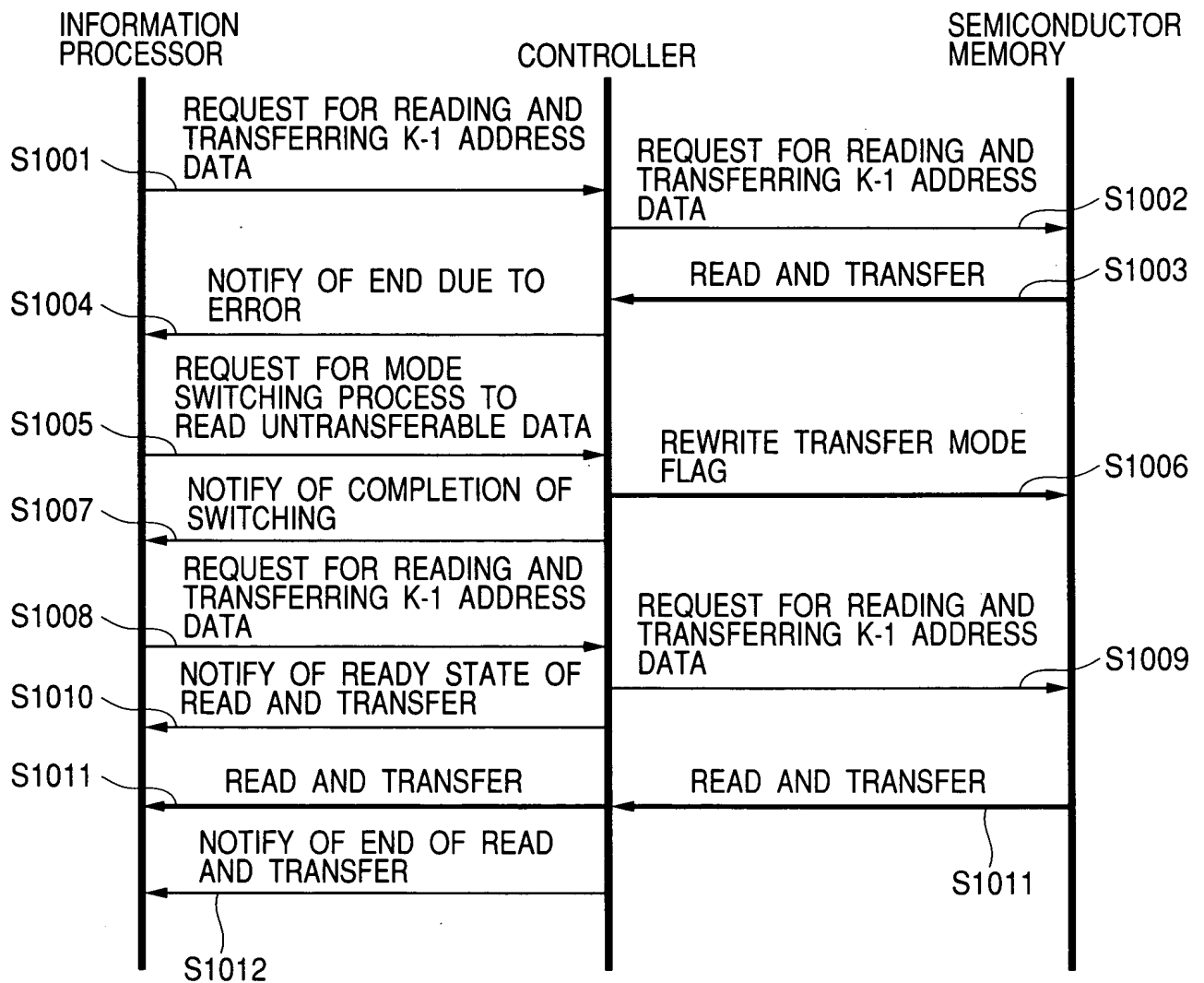
FIG. 29

FIG. 30

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SEMICONDUCTOR MEMORY		
ADDRESS	DATA STORAGE AREA	DATA AREA FOR ERROR DETECTION
0	USER DATA (0)	DETECTION DATA (0)
1	USER DATA (1)	DETECTION DATA (1)
⋮	⋮	⋮
k-1	USER DATA (k-1)	DETECTION DATA (k-1)
k	USER DATA (k)	DETECTION DATA (k)
⋮	⋮	⋮
n-1	USER DATA (n-1)	DETECTION DATA (n-1)
n	TRANSFER INVALID FLAG	DETECTION DATA (n)

FIG. 31

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SEMICONDUCTOR MEMORY		
ADDRESS	DATA STORAGE AREA	DATA AREA FOR ERROR DETECTION
0	USER DATA (0)	DETECTION DATA (0)
1	USER DATA (1)	DETECTION DATA (1)
⋮	⋮	⋮
k-1	USER DATA (k-1)	DETECTION DATA (k-1)
k	USER DATA (k)	DETECTION DATA (k)
⋮	⋮	⋮
n-1	USER DATA (n-1)	DETECTION DATA (n-1)
n	TRANSFER VALID FLAG	DETECTION DATA (n)

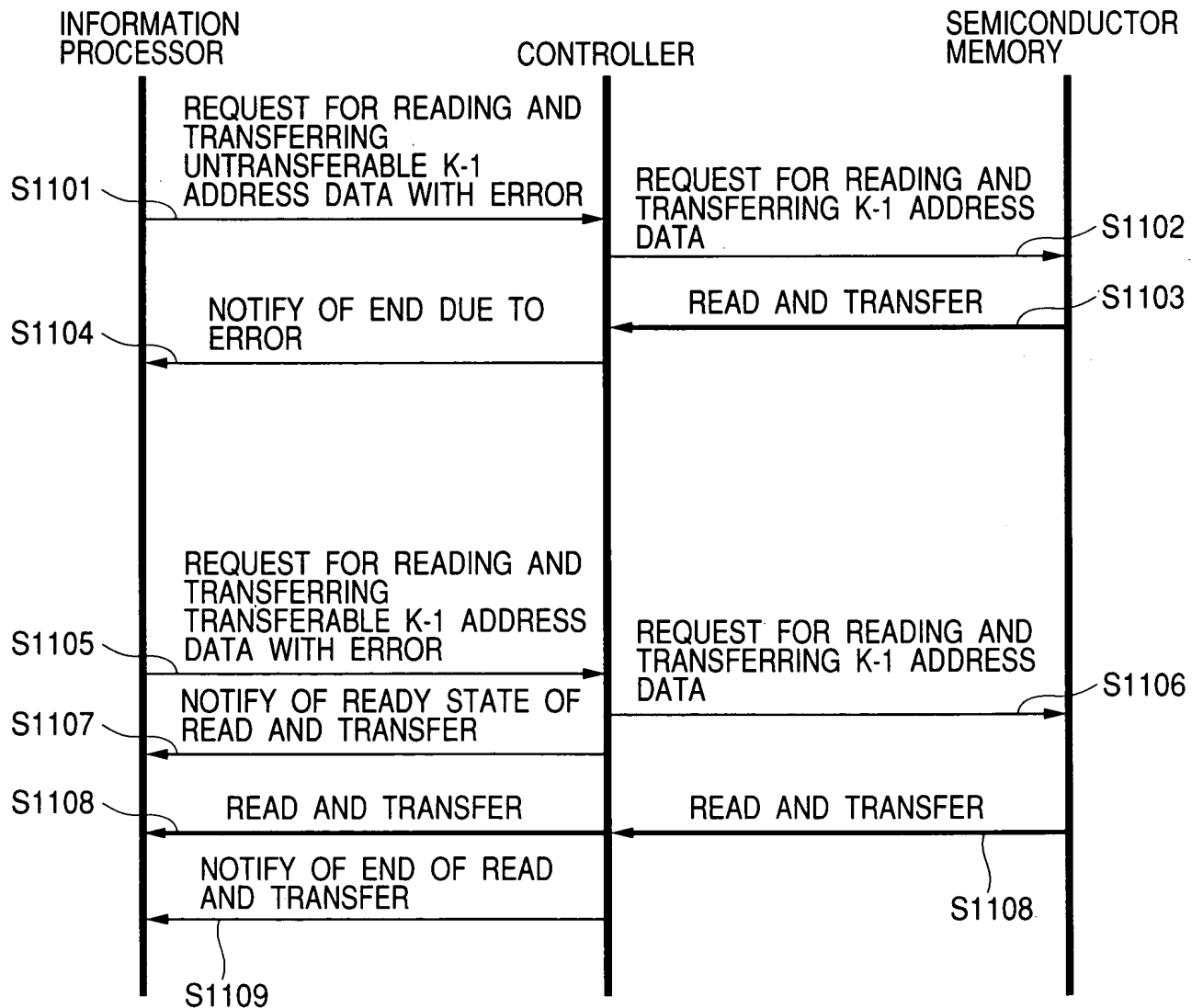
FIG. 32

FIG. 33

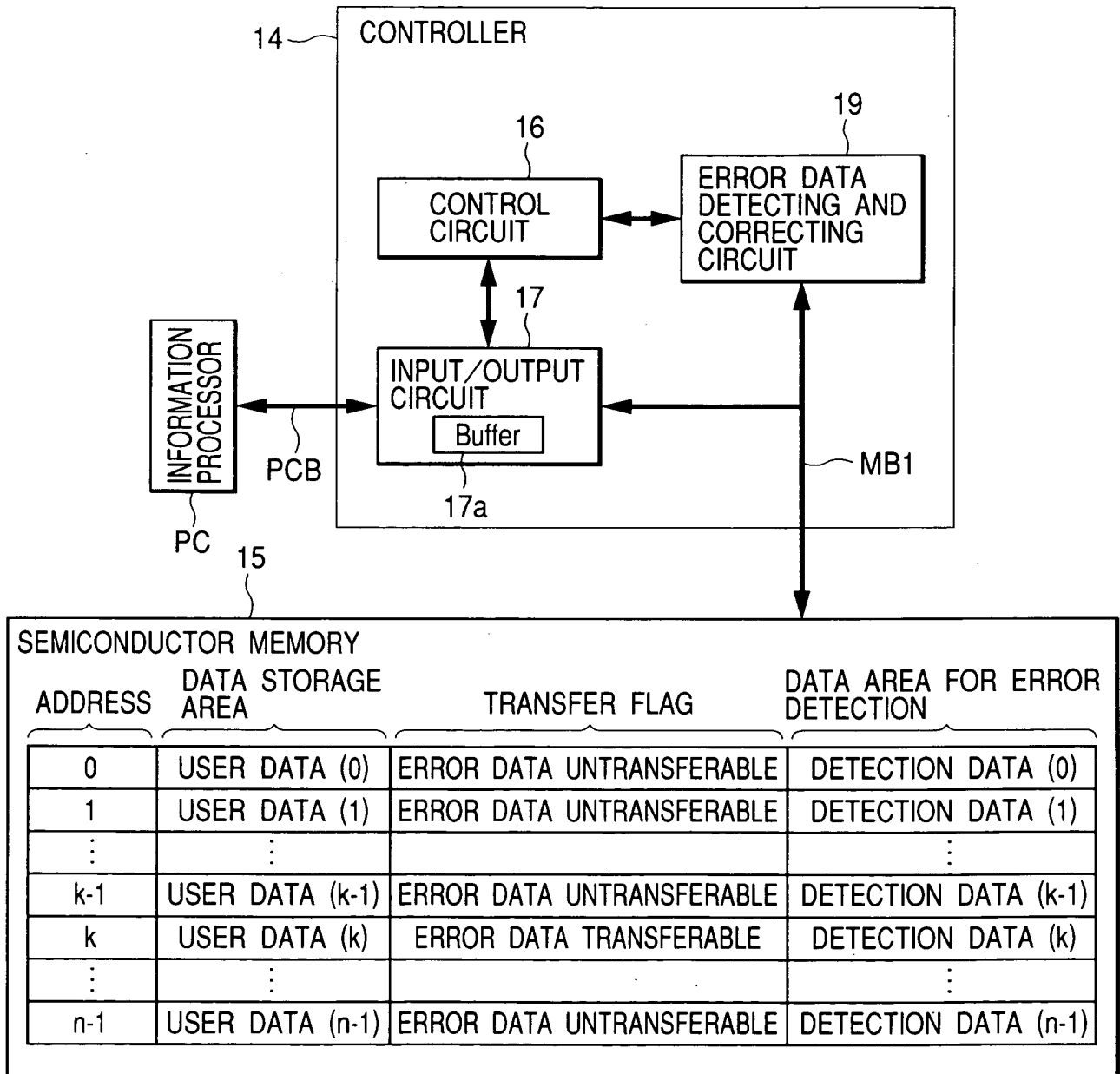


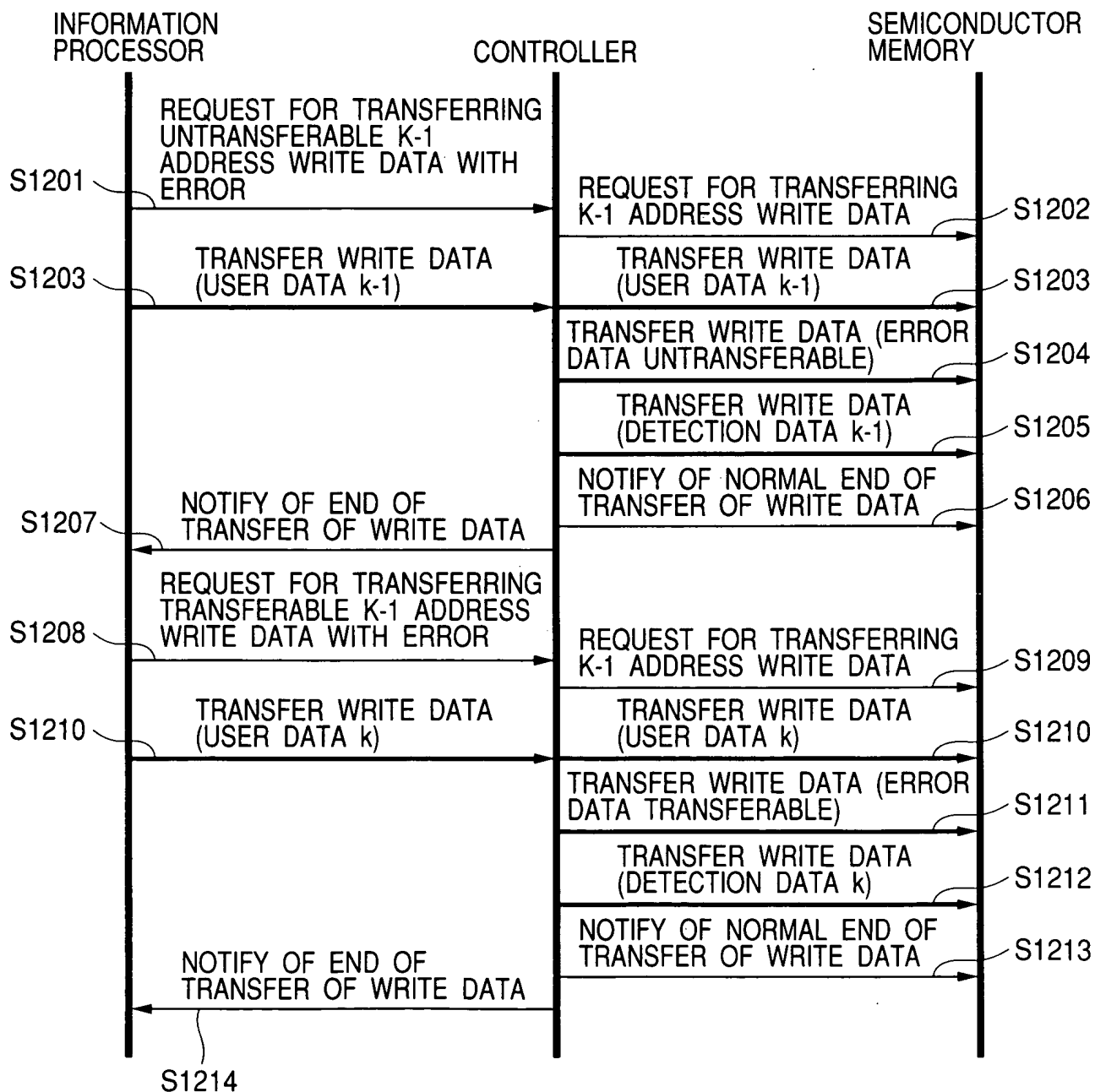
FIG. 34

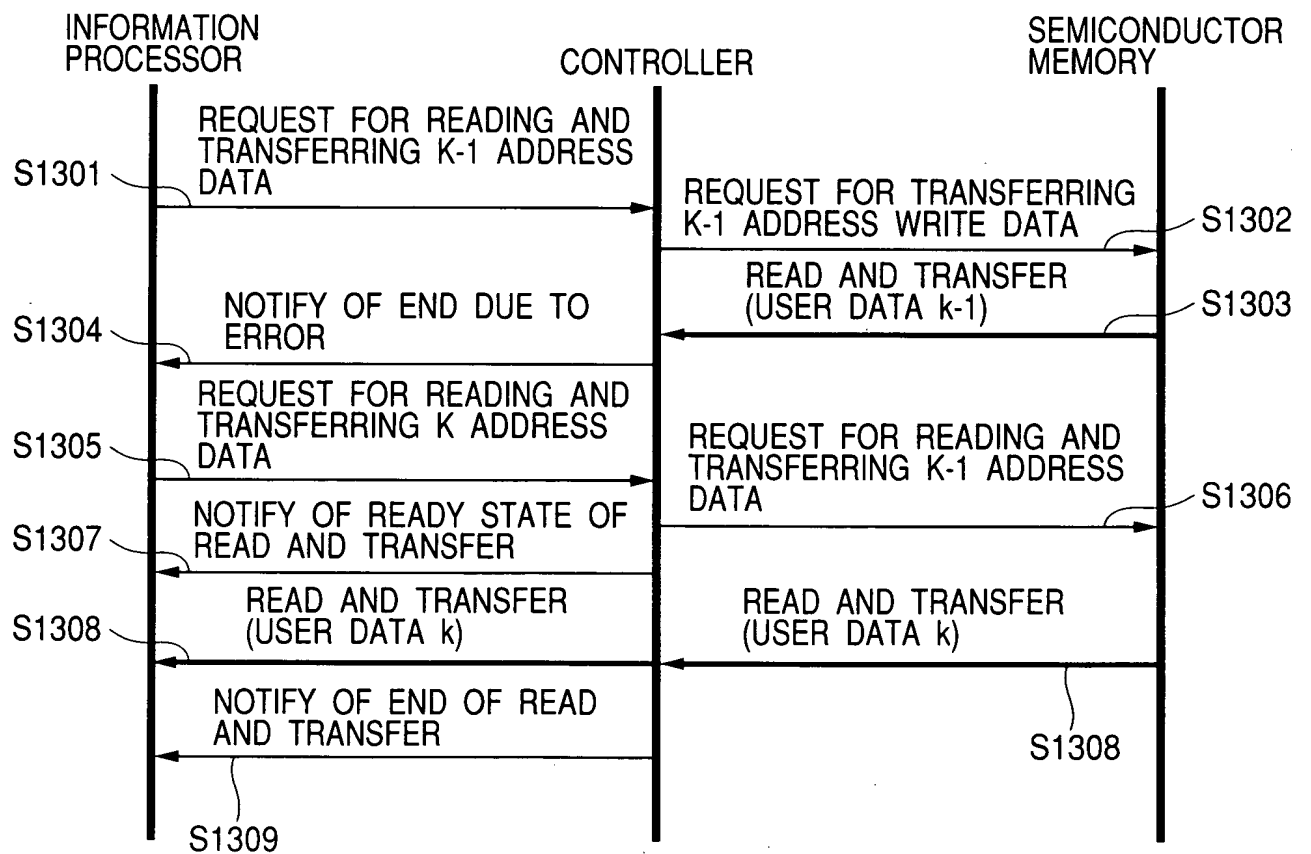
FIG. 35

FIG. 36